CLAIMS

1. An interconnect substrate over which an interconnect pattern is formed, comprising:

a first portion; and

a second portion to be superposed on the first portion,

wherein the first portion has an end part as a positioning reference; and

wherein the second portion has a shape so as to be superposed on the first portion except the end part.

2. The interconnect substrate as defined in claim 1,

wherein the end part as the positioning reference includes two edges which are perpendicular to each other.

3. The interconnect substrate as defined in claim 1,

wherein the first portion comprises a rectangular body section and a projected section which extends from at least one edge of the body section and includes the end part.

4. The interconnect substrate as defined in claim 3,

wherein the projected section is a region determined by:

an edge which is a boundary between the projected section and the body section;

a first edge which is perpendicular to the edge as a boundary; and

a second top edge which is parallel to the edge as a

boundary,

wherein the end part as a positioning reference includes the first and second edges.

5. The interconnect substrate as defined in claim 4,

wherein the body section of the first portion includes an edge having no projected section; and

wherein the second portion is disposed adjacent to the edge having no projected section.

6. The interconnect substrate as defined in claim 4,

wherein the second portion has a depressed section facing the projected section of the first portion.

7. The interconnect substrate as defined in claim 6,

wherein the first portion has a plurality of the end parts as positioning references; and

wherein at least one of the end parts is formed from an area in the body section other than an area from which the projected section extends.

8. The interconnect substrate as defined in claim 2,

wherein the first portion is larger than the second portion; and

wherein the two edges which are perpendicular to each other form a corner section of the first portion.

9. The interconnect substrate as defined in claim 2,

wherein the first portion has a depressed end part including the two edges which are perpendicular to each other and have an right angle.

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10. The interconnect substrate as defined in claim 1,

wherein a plurality of holes are formed in the end parts.

11. The interconnect substrate as defined in any one of claims 1 to 10,

wherein the second portion continuously extends from the first portion.

12. The interconnect substrate as defined in any one of claims 1 to 10,

wherein the second portion is separated from the first portion; and

wherein the first and second portions are connected by the interconnect pattern.

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13. A semiconductor device comprising:

at least one semiconductor chip; and

a substrate which has a first portion and a second portion to be superposed on the first portion, and on which the semiconductor chip is mounted,

wherein the first portion includes an end part as a positioning reference; and

wherein the second portion has a shape which avoids being superposed over the end part of the first portion.

14. The semiconductor device as defined in claim 13, wherein a plurality of external terminals are provided in the first portion.

15. The semiconductor device as defined in claim 13, wherein the interconnect substrate as defined in any one of claims 1 to 10 is used as the substrate.

16. A circuit board over which is mounted the semiconductor device as defined in claim 13 or 14.

17. An electronic instrument provided with the semiconductor device as defined in claim 13 or 14.

18. A method of fabricating a semiconductor device, comprising the steps of:

mounting at least one semiconductor chip over the interconnect substrate as defined in any one of claims 1 to 10; and

superposing the second portion on the first portion of the interconnect substrate.

19. A method of inspecting a semiconductor device, comprising the steps of:

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positioning the semiconductor device as defined in claim 13 or 14 by using a plurality of end parts as positioning references; and

inspecting electrical characteristics of the semiconductor device.

20. A method of mounting a semiconductor device comprising the steps of:

positioning the semiconductor device as defined in claim 13 or 14 by using a plurality of end parts as positioning references; and

mounting the semiconductor device on a circuit board.